IN THE CLAIMS

Per the revised amendment practice, a complete listing of all claims in the application follows.

Claims 1-46. (Cancelled)

47. (Currently amended) ~~The circuit in claim 45, further comprising~~ A circuit for a semiconductor chip including a memory array and an address latch, wherein said chip is configured to electrically communicate with a terminal of a tester, said circuit comprising:

a comparator on said semiconductor chip coupled to said memory array and to said terminal of said tester, wherein said comparator is configured to receive a first data value from said memory array and a second data value from said terminal and further configured to transmit a signal based upon a lack of identity between said first and second data values;

a register coupled to said address latch and to said comparator, wherein said first data value is associated with an address transmitted by said address latch, and wherein said register is configured to store said address in response to receiving said signal from said comparator, wherein said register is configured to store less than two addresses at one time, and wherein said register is configured to preferably store a later address corresponding to a later transmission of said signal over a prior address corresponding to a prior transmission of said signal; and

an output circuit comprising:

an inverter coupled to said memory array[[;]] ,

a first transistor electrically interposed between said inverter and a positive voltage source and configured to turn off during a test mode for said semiconductor chip[[;]] , and

a second transistor electrically interposed between said inverter and ground and configured to turn off during said test mode.

48. (Original) The circuit in claim 47, further comprising a buffer electrically interposed between said terminal and said comparator.

49. (Original) The circuit in claim 48, wherein said comparator comprises an exclusive nor gate.

Claims 50-53 (Cancelled).

54. (New) A circuit for a semiconductor chip including a memory array and an address latch, wherein said chip is configured to electrically communicate with a terminal of a tester, said circuit comprising:

a comparator on said semiconductor chip coupled to said memory array and configured to couple to said terminal of said tester, wherein said comparator is configured to receive a first data value from said memory array and a second data value from said terminal and further configured to transmit a signal based upon a lack of identity between said first and second data values;

a register coupled to said address latch and to said comparator, wherein said first data value is associated with an address transmitted by said address latch, and wherein said register is configured to store said address in response to receiving said signal from said comparator, wherein said register is configured to store less than two addresses at one time, and wherein said register is configured to preferably store a later address corresponding to a later transmission of said signal over a prior address corresponding to a prior transmission of said signal; and

an output circuit comprising:

an inverter coupled to said memory array,

a first transistor electrically interposed between said inverter and a positive voltage source and configured to turn off during a test mode for said semiconductor chip, and

a second transistor electrically interposed between said inverter and ground and configured to turn off during said test mode.

55. (New) The circuit in claim 54, wherein said inverter is configured to couple to said terminal.

56. (New) The circuit in claim 55, wherein:

said inverter is further configured to transmit an output value to said terminal during a non-test mode, wherein said output value is based on data stored in said memory array;

said first transistor is configured to turn on in response to entering said non-test mode; and

said second transistor is configured to turn on in response to entering said non-test mode.

57. (New) The circuit in claim 56, wherein said output value is an inverse of said data stored in said memory array.